

Claim Amendments

1 1-19. (canceled).

1 20. (original) A comparator comprising;

2 an input amplifier including:

3 a first pair of input transistors having a first transistor type, each of
4 the first pair of input transistors being coupled to a
5 corresponding input terminal operable to receive a
6 respective input signal;

7 a second pair of input transistors having a second transistor type,
8 each of the second pair of input transistors being coupled to
9 a respective one of the corresponding input terminals;

10 a first current mirror coupled to the first pair of input transistors and
11 operable to sum a first pair of input amplifier output signals and
12 provide at least a portion of a comparator output signal on a
13 comparator output terminal;

14 a second current mirror coupled to the second pair of input transistors and
15 operable to sum a second pair of input amplifier output signals and
16 provide at least another portion of the comparator output signal on
17 the comparator output terminal;

18 a first hysteresis transistor including a first hysteresis transistor input
19 terminal coupled to the comparator output terminal and operable to
20 supply a first hysteresis current to at least one of the first current
21 mirror and the second current mirror; and

22 a second hysteresis transistor including a second hysteresis transistor
23 input terminal coupled to the comparator output terminal and
24 operable to supply a second hysteresis current to at least one of
25 the first current mirror and the second current mirror.

1 **21. (new) The comparator of claim 20, wherein the comparator is**
2 **integrated within a programmable analog integrated circuit.**

1 **22. (new) The programmable analog integrated circuit of claim 21, wherein**
2 **the integrated circuit comprises:**
3 **a plurality of analog circuit blocks;**
4 **a plurality of comparators; and**
5 **an analog routing pool coupled to the analog circuit blocks and**
6 **comparators.**

1 **23. (new) A comparator comprising;**
2 **an input amplifier including:**
3 **a first pair of input transistors having a first transistor type, each of**
4 **the first pair of input transistors being coupled to a**
5 **corresponding input terminal operable to receive a**
6 **respective input signal;**
7 **a second pair of input transistors having a second transistor type,**
8 **each of the second pair of input transistors being coupled to**
9 **a respective one of the corresponding input terminals;**
10 **a summing stage coupled to the input amplifier and operable to sum input**
11 **amplifier output signals and provide a comparator output signal on**
12 **a comparator output terminal; and**
13 **a hysteresis feedback stage coupled to the comparator output terminal**
14 **and operable to supply a hysteresis current to the summing stage.**

1 **24. (new) The comparator of claim 23, wherein the summing stage**
2 **comprises:**
3 **a first current mirror coupled to the first pair of input transistors and**
4 **operable to sum a first pair of input amplifier output signals and**
5 **provide at least a portion of the comparator output signal on the**
6 **comparator output terminal; and**

7 **a second current mirror coupled to the second pair of input transistors and**
8 **operable to sum a second pair of input amplifier output signals and**
9 **provide at least another portion of the comparator output signal on**
10 **the comparator output terminal.**

1 **25. (new) The comparator of claim 23, wherein the hysteresis stage**
2 **comprises:**
3 **a first hysteresis transistor including a first hysteresis transistor input**
4 **terminal coupled to the comparator output terminal and operable to**
5 **supply a first hysteresis current to the summing stage; and**
6 **a second hysteresis transistor including a second hysteresis transistor**
7 **input terminal coupled to the comparator output terminal and**
8 **operable to supply a second hysteresis current to the summing**
9 **stage.**

1 **26. (new) The comparator of claim 23, wherein the comparator is**
2 **integrated within a programmable analog integrated circuit.**

1 **27. (new) The programmable analog integrated circuit of claim 26, wherein**
2 **the integrated circuit comprises:**
3 **a plurality of analog circuit blocks;**
4 **a plurality of comparators; and**
5 **an analog routing pool coupled to the analog circuit blocks and**
6 **comparators.**

1 **28. (new) A comparator comprising;**
2 **an input amplifier;**
3 **a summing stage including:**
4 **a first current mirror coupled to the input amplifier and operable to**
5 **sum a first pair of input amplifier output signals and provide**
6 **at least a portion of the comparator output signal on a**
7 **comparator output terminal; and**

8 a second current mirror coupled to the input amplifier and operable
9 to sum a second pair of input amplifier output signals and
10 provide at least another portion of the comparator output
11 signal on the comparator output terminal; and
12 a hysteresis feedback stage coupled to the comparator output terminal
13 and operable to supply a hysteresis current to the summing stage.

1 29. (new) The comparator of claim 28, wherein the hysteresis stage
2 comprises:
3 a first hysteresis transistor including a first hysteresis transistor input
4 terminal coupled to the comparator output terminal and operable to
5 supply a first hysteresis current to at least one of the first current
6 mirror and the second current mirror of the summing stage; and
7 a second hysteresis transistor including a second hysteresis transistor
8 input terminal coupled to the comparator output terminal and
9 operable to supply a second hysteresis current to at least one of
10 the first current mirror and the second current mirror of the
11 summing stage.